In the Claims:

1. (Currently Amended) A vertical dynamic random access memory (DRAM) cell device fabricated within a trench region in a substrate, the trench region having first and second opposing substantially vertical edges extending from the device surface, the vertical DRAM cell comprising:

(a) a storage capacitor formed within the trench region for storing electrical charge;

(b) a transistor formed within the trench region above the storage capacitor;

(c) a buried strap having a top surface formed proximate to the first vertical edge between the storage capacitor and the transistor, the buried strap electrically coupling the storage capacitor and the transistor; and

(d) an isolation collar region having a bottom edge, said collar region formed proximate to the second vertical edge of the trench, and said bottom edge extending past said transistor, but no further than about 100nm below said top surface of said buried strap~~the isolation collar extending the length of the transistor~~.

2. (Currently Amended) The cell device according to claim 1, further comprising a trench top oxide (TTO) region comprising a bottom surface, the bottom surface located above said [[a]] top surface of the buried strap, wherein the trench top oxide and the buried strap are located between the transistor and the storage capacitor.

3. (Currently Amended) The cell device according to claim 2, wherein the top surface ~~portion~~ of the buried strap is vertically separated from the bottom surface of the trench top oxide by about 150 to 450 nm.

4. (Currently Amended) The cell device according to claim 1 [[3]], wherein said bottom edge of the isolation collar region extends ~~has a bottom edge, the bottom edge extending~~ below the vertical location of the buried strap top surface between about 50 to 100nm~~by about 50-1000~~.

5. (Currently Amended) The cell device according to claim 1 [[3]], wherein said bottom edge of the isolation collar region is ~~has a bottom edge, the bottom edge~~ vertically separated from the top surface of the trench ~~buried strap~~ by between about 500-1000nm~~50-100 nm~~.

6. (Original) The cell device according to claim 4, wherein the buried strap comprises a one-sided strap.

7. (Original) The cell device according to claim 6, wherein the one-sided strap has a vertical dimension in the range of about 30 to 150 nm, and a lateral dimension in the range of about 50-100 nm.

8. (Currently Amended) The cell device according to claim 1 [[5]], wherein the buried strap comprises a one-sided strap.

9. (Original) The cell device according to claim 8, wherein the one-sided strap has a vertical dimension in the range of about 30 to 150 nm, and a lateral dimension in the range of about 50 to 100 nm.

10. (Currently Amended) A buried strap for electrically connecting a transistor and a storage capacitor in a vertical dynamic random access memory (DRAM) cell device formed within a semiconductor substrate, said substrate defining ~~and having~~ a trench with first and second opposing vertical edges, the buried strap comprising: an electrically conducting region formed within the trench, the electrically conducting region formed proximate to the first opposing edge between the transistor and storage capacitor, and laterally displaced from an isolation region extending from the semiconductor substrate surface along the second opposing vertical edge and terminating at a bottom [[an]] edge no lower than about 50-100nm below a top surface of the buried strap.~~electrically conducting region, the buried strap formed at or below edge of the isolation region.~~

11. (Currently Amended) The buried strap according to claim 10, ~~wherein the electrically conducting region~~ being formed proximate [[to]] the first opposing edge and [[is]] laterally separated from the second opposing edge by about 50-110 nm.

12. (Cancel)

13. (Currently Amended) The buried strap according to claim 10, wherein the ~~shallow trench~~ isolation region has a depth no greater than about 250-350 nm.

14. (Cancel)

15. (Currently Amended) The buried strap according to claim 10 [[12]], wherein the ~~shallow trench~~ isolation region comprises an oxide collar for electrically isolating the transistor and the storage capacitor in the vertical DRAM cell device from potential cross talk with an adjacent DRAM cell device.

16. (Original) The buried strap according to claim 10, wherein the electrically conducting region comprises undoped polysilicon.

17. (Original) The buried strap according to claim 10, wherein the electrically conducting region comprises doped polysilicon.

18.-32. (Cancel)